



# Sigma-Delta Stereo ADCs for High Performance Audio



The Intrinsic Sigma-Delta Stereo ADCs for High Performance Audio ( $\Sigma\Delta$ -ADC-HPA™) are part of the larger offering of Sigma-Delta IP available from Intrinsic. For a complete list of datasheets for all the Sigma-Delta based IP plus an overview of the concepts and benefits of Sigma-Delta (or sometimes called Delta-Sigma) modulators and data converters visit us online at <http://www.intrinsic.com/intrinsic-ip/sigma-delta/>

The family of  $\Sigma\Delta$ -ADC-HPAs are generated utilizing proprietary, patent-pending techniques within the Intrinsic SDM Refinery™ toolset. A design methodology that is geared towards a digital CMOS process helps reduce cost, die size and power consumption. A high Signal to Noise Ratio (SNR) is achieved by pushing the frequency of the quantization noise outside the band of interest. The challenge in Sigma-Delta ADC design is the “shaping” of this noise, which is characterized by the Noise Transfer Function (NTF), and the design of efficient filters to attenuate the noise. The SDM Refinery automates this process: The engineer specifies an Over-Sampling Ratio (OSR), quantization levels, order of complexity and SDM Refinery creates the desired ADC. More information on SDM Refinery™ can be found at <http://www.intrinsic.com/intrinsic-ip/sigma-delta/>

## Intrinsic $\Sigma\Delta$ -ADC-HPAs are:

- Perfect for high quality audio applications that such as:
  - ▶ Professional Audio and Studio Recording/Mixing
  - ▶ Musical Instruments
  - ▶ Professional and Consumer Digital Audio Recorders
  - ▶ Audio Feedback Controls (Professional, Home, Auto, etc)
  - ▶ Multimedia Systems
  - ▶ Audio Sensors (aka Frequency Sensors)
- Silicon proven architectures can be incorporated in a variety of CMOS-based silicon technologies
  - ▶ TSMC, SMIC, UMC and Chartered (but portable to any appropriate vendor)
  - ▶ .130 $\mu\text{m}$ , .180 $\mu\text{m}$  and .250 $\mu\text{m}$  and 90nm
- Available in 16, 20 and 24-bit resolutions
- Available in 3<sup>rd</sup> and 4<sup>th</sup> Order  $\Sigma\Delta$  Modulation Complexity (others available upon request)
- Able to achieve a Signal-to-Noise Ratio (SNR) of 105db
- Optimized for multi-channel functionality
- Compact design resulting in small die area
- Very low in power consumption with a customizable Low Power Mode
- Highly tunable for each application
- Available as RTL and GDSII as well as RTL and Behavioral System models in industry standard formats such as Verilog-A or Simulink



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