



# Programmable Sigma-Delta ADC

## SNR – Power – Bandwidth Tunable A/D Converter

### **BENEFITS**

- In-System Programmability allows for multiple modes
- Optimize each mode by specifying trade-offs between:
  - Signal-to-Noise Ratio
  - Power
  - Bandwidth
- Capable of achieving:
  - Very Low Power
  - High Performance
  - High Precision

### **APPLICATIONS**

- Precision Data Conversions
- High Performance Audio

### **FEATURES**

- Differential VREF inputs
- Common Mode Voltage range:  $0.85V \pm 0.1V$
- Third-order two-bit Sigma-Delta Modulator (SDM) with 0 - 100KHz bandwidth, and no idle tones
- Incorporates a high-performance DEM logic
- Analog (AVDD) Supply voltage:  $1.8V \pm 10\%$
- Digital (DVDD) Supply voltage:  $1.8V \pm 10\%$
- Low power consumption: 1.8 - 5mW (in-system programmable)
- High performance: 101 - 110dB (in-system programmable)
- SDM enable allows for granular control of power consumption
- Specification driven temperature range: 0oC to +100oC (junction temperature). In this temperature range, the IP block can meet all the performance specifications.
- Operational temperature range: -40oC to +125oC (junction temperature). In this temperature range, the IP block should be functional, but it may or may not meet the performance specifications.
- Technology: UMC 0.18 $\mu$ m CMOS process with MiM capacitors
- Die Size: approximately 1.5mm<sup>2</sup> (excluding pads)

### **IP OVERVIEW**

The Intrinsic Programmable Sigma-Delta Modulator (SDM) based ADC is a proprietary IP block, based on our patented SDM development process, with six programmable bandwidth settings. It includes a third-order switched-capacitor sigma-delta modulator employing 4-level (2-bit) quantization. Furthermore, the IP block includes a high-performance proprietary Dynamic Element Matching (DEM) logic to greatly reduce the inevitable adverse effects of multi-bit quantization.

The Intrinsic SDM ADC is implemented using UMC 0.18  $\mu$ m CMOS process with MiM (Metal-insulator-Metal) capacitors. There are six possible bandwidth settings for the IP, which can be configured using a three-bit digital input signal, SDM\_BW[2:0]. The maximum input signal to the IP block is a 2.0 V<sub>pp</sub> (peak-to-peak voltage) differential voltage with 0.85 Volt common-mode voltage (V<sub>cm</sub>). Power supply voltages are VDDA=1.8 Volt and VSSA=0 Volt, both for analog and digital circuits.

